

ABSTRACT

A DSP superscalar architecture employing dual multiply accumulate pipelines. Dual MAC pipelines allow for a seem less transition between established RISC instruction sets and extended DSP instructions sets. Relocatable opcodes are provide to allow further extensions of RISC instruction sets. The DSP superscalar architecture also provides memory pointers with hardware circular buffer support, an interruptible and nested zero-overhead loop counter, and prioritized low-overhead interrupts.